Proceedings of the 30th International Symposium on Power Semiconductor Devices & ICs
May 13-17, 2018, Chicago, USA

Si Wafer Technology for Power Devices

A Review and Future Directions

Norihisa Machida
Customer Product Engineering Department, Technology Division
SUMCO Corporation
Kouhoku, Saga, Japan
machida@sumcosi.com

***Abstract*—Silicon wafers have been widely used in semiconductor devices for years. Their characteristics have been improved by untiring development efforts to meet power device manufacturers' requirements such as lowering substrate resistivity for Power MOSFET and reducing resistivity variation for IGBT. As future directions, by utilizing advantages of silicon wafers, adoption of MCZ grown bulk silicon wafers for low and middle voltage IGBT and introduction of 300mm size silicon wafers will proceed.**

Keywords— silicon wafer, Power MOSFET, IGBT, MCZ, 300mm

I. INTRODUCTION

Silicon wafers have been widely used for semiconductor devices including memory, logic, image sensors, and power devices for a long time. In 2017, worldwide annual consumption of silicon wafers reached 11,810 million square inches in accumulated area [1] or equivalently more than 235 million pieces of 200mm size wafers. SUMCO is a leading silicon wafer manufacturer which has been supplying wide range products to major device manufacturers based on advanced R&D activities [2].

For today's power devices, various silicon wafers are used on the basis of required breakdown voltage for specific power devices. For Power MOSFET devices, epitaxial wafers are mainly used to secure uniform quality active layer. For high breakdown voltage required IGBT, bulk silicon wafers by Floating zone (FZ) crystal growing method are used to secure defect-free active layer. And for lower breakdown voltage IGBT, bulk silicon wafers by Magnetic field applied Czochralski (MCZ) crystal growing method are recently adopted by various device manufactures for stable, large volume material procurement (Fig. 1). In addition, MCZ bulk silicon wafers can provide the device manufacturers with an option to enlarge the wafer size to 300mm. Technical issues of silicon wafers for power devices are basically improvement of switching characteristics: reducing on-resistance for Power MOSFET and saturation voltage between collector and emitter (Vce(sat)) for IGBT.

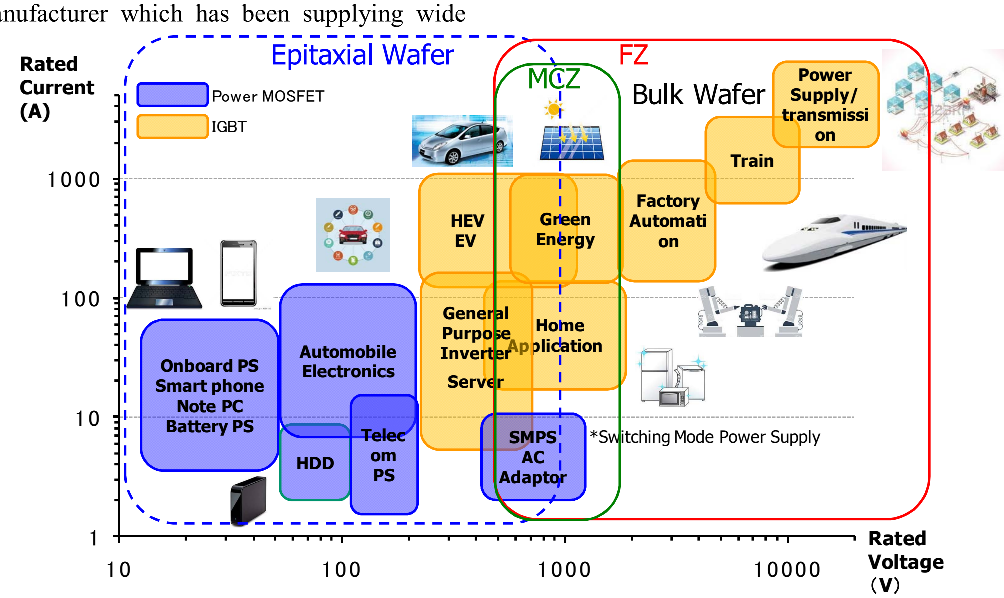

Fig. 1. Silicon wafers used for power devices by rated voltage and rated current

II. POWER MOSFET

For Power MOSFET, specific on-resistance Rsp could be divided to three components: channel on-resistance (Rch), epitaxial layer on-resistance (Repi), and substrate on-resistance (Rsub) (1).

$$Rsp = Rch + Repi + Rsub \qquad (1)$$

Substrate resistivity, Rsub has higher contribution ratio to reducing the specific on-resistance in case of thinner epitaxial layer low voltage Power MOSFET [3].

To lower resistivity of negative conductivity type bulk silicon wafers, arsenic has been used as a dopant until facing a physical limitation of stable single crystal growth around 1.6 mΩcm level due to the cellular growth. In case of heavy doping, crystal growth would face a constitutional supercooling that could induce the cellular growth and consequent structure loss of single crystal. The constitutional supercooling condition can be described by (2)[4].

$$G_L/V \leqq mC_0/D \cdot (1-k_0)/k_0 \qquad (2)$$

where G_L is temperature gradient of silicon melt; V is silicon crystal growth rate; m is depression of freezing point; C_0 is initial dopant concentration; D is diffusion coefficient of dopant in the silicon melt; and, k_0 is segregation coefficient of dopant.

Instead of arsenic ($k_0 = 0.3$), phosphorous doping which has larger segregation coefficient ($k_0 = 0.35$) has been utilized to grow even lower resistivity bulk silicon crystals for low voltage Power MOSFET devices (Fig. 2). Today, by optimizing the factors described in (2), phosphorous doped silicon wafers with lower than 0.7 mΩcm are available in market. Further lower resistivity bulk silicon wafers are under development.

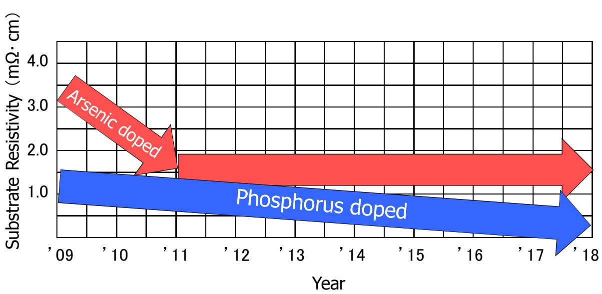

Fig. 2. Trend of substrate resistivity for low voltage Power MOSFET

III. IGBT

Since IGBT modules used for industry, automotive, and electric train consist of a set of IGBT chips, individual IGBT chip's characteristics such as Vce(sat) should be controlled within desired variation range. The resistivity variation that affects Vce(sat) needs to be controlled in a single wafer and among silicon wafers. The neutron transmutation doping (NTD) has been used to obtain controlled variation of resistivity. Meanwhile, long leading time and unstable nuclear facility availability promoted resistivity variation improvement with so-called normal doping techniques for bulk silicon wafers. The capabilities of resistivity variation using gas doping for FZ silicon wafers and phosphorous doping for MCZ silicon wafers are getting to the same or better level comparing with NTD silicon wafers today (Fig. 3).

Although MCZ bulk silicon wafers certainly contain some level of oxygen and crystal originated defects, collaborating efforts with device manufacturers and process tuning enabled adoption of MCZ bulk silicon wafers for low and middle breakdown voltage IGBT today.

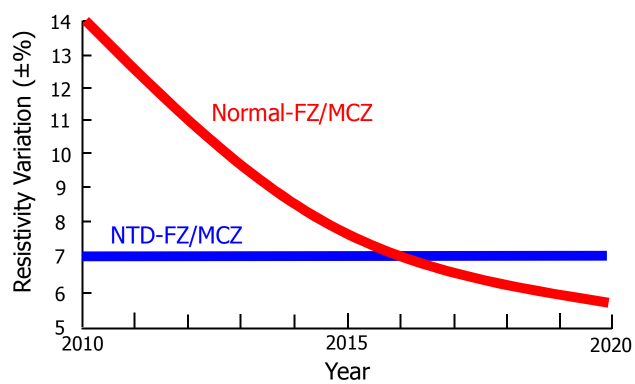

Fig. 3. Trends of resistivity variation of FZ and MCZ silicon wafers by doping method

IV. FUTURE DIRECTIONS

As future directions, silicon wafer advantages of higher productivity and lower cost for high volume market segments will be moreover utilized. Specifically, further adoption of MCZ bulk silicon wafers and 300mm wafers will continue and expand for years. Fig. 4 shows our image of silicon wafers transition for IGBT in near future. More MCZ bulk silicon wafers including 300mm size will support the vigorously growing market. Likewise, there could be a good chance to adopt more 300mm MCZ substrate for Power MOSFET devices in future.

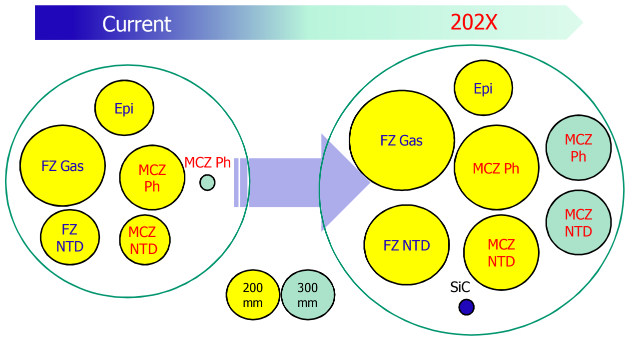

Fig. 4. An image of silicon wafers transition for IGBT

REFERENCES

[1] SEMI press release of February 6, 2018, http://www.semi.org/jp/jp/node/81221

[2] Hisashi Furuya, Silicon Wafers for Advanced Devices,The 7th International Symposium on Advanced Science and Technology of Silicon Materials, Nov. 21-25 , 2016

[3] International Rectifier Application Note AN-1084, Power MOSFET Basics, Vrej Barkhordarian, https://www.infineon.com/dgdl/mosfet.pdf?fileId=5546d462533600a4015357444e913f4f

[4] W.A.Tiller, K.A.Jackson, J.W.Rutter, B.Chalmers, Acta Metall. 1, 428 (1953)